Selecting and Using High-Precision Digital-to-Analog Converters

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Many applications, including precision instrumentation, industrial automation, medical devices, and automated test equipment, require high-precision digital-to-analog conversion. In circuits that require accuracy of better than about ±15ppm, or ±1LSB at 16-bit resolution, designers have traditionally been forced to use extensive calibration to maintain accuracy over all conditions. New high-precision DACs make it possible to achieve ±4ppm accuracy, or ±1LSB at 18-bit resolution using a single monolithic DAC without calibration. In this article we will consider the issues involved in selecting and using high-precision digital-to-analog converters.

The DAC architecture affects both the specifications of the DAC and the demands it places on the board designer. Careful consideration of the effects of the power supply, reference, and output amplifier on the DAC is required to achieve the best performance.

Oversampled or Delta-Sigma DACs

An oversampled or delta-sigma DAC uses a low-resolution DAC, normally just 1 bit, preceded by a noise-shaping digital modulator and followed by an analog low-pass filter. The most accurate commercially available delta-sigma DACs achieve ±15ppm accuracy, but require 15ms to settle and suffer a relatively high 1µV/√Hz noise density. Other available oversampled DACs achieve settling in 80µs but suffer poor INL of about 240 ppm.

Composite DACs

It is possible to construct a high-resolution composite DAC by combining two lower resolution monolithic DACs. Note that overlap between the resolution of the coarse DAC and the range of the fine DAC is required to ensure that all desired output voltages are realizable. The accuracy and drift of the coarse DAC will normally limit the end accuracy of the composite DAC, so increased precision requires characterization and software correction of the composite DAC transfer function. Frequent calibration may also be required to correct for drift due to variations with temperature, time, humidity and mechanical stress. Figure 1 shows an example from Linear Technology Application Note 86 in which an ADC is used in a feedback loop to continually adjust two 16-bit DACs to achieve ±1ppm accuracy.
Resistor String DACs

A resistor string DAC uses a series resistive divider with $2^N$ tap points to achieve N-bit resolution. Monolithic 16-bit DACs that use resistor string architectures normally contain a lower resolution resistor string DAC with a sub-ranging DAC used to interpolate between the elements of the string to achieve 16-bit resolution. One advantage of this string-plus-interpolator approach is that the DAC output is inherently monotonic without trimming or calibration.

The reference input impedance of such DACs is typically high (50–300kΩ) and independent of input code, making it possible to use an unbuffered reference. Since the output impedance of the resistor string varies with input code, most resistor string DACs include integrated output buffer amplifiers to drive resistive loads.

Although the DNL of resistor string DACs is inherently very good, the INL is determined by the matching of the series resistive elements and can be difficult to control due to the large number of independent elements involved. Until recently the accuracy of such DACs has been limited to about ±180ppm. Recent advances have enabled accuracies of up to ±60ppm. For example, the LTC2656 integrates 8 DAC channels in a 4mm x 5mm package with ±4LSB max INL at 16-bit resolution.
Resistive Ladder or R-2R DACs

Resistive ladder or R-2R DACs use a three terminal structure like that shown in Figure 2, with resistors switched between terminals A and B. Note that the impedances at terminals A and B are highly code dependent, while terminal C has a fixed impedance. The matching of the resistors and switches will affect the monotonicity and accuracy of the structure. Such DACs are normally trimmed or factory calibrated, and monolithic 16-bit resistive ladder DACs with ±1LSB INL and DNL have long been commonly available.

![Resistive ladder DAC structures](image)

Voltage Output R-2R DACs

One common style of R-2R DAC uses terminal C as the DAC output voltage, with terminal A connected to the reference and terminal B connected to ground. The output impedance is constant relative to the input code, making it possible to drive resistive loads unbuffered. For example, the LTC2641 16-bit DAC can drive a 60kohm load unbuffered while maintaining ±1LSB INL and DNL and consuming less than 200μA supply current.

One disadvantage of this approach is that the reference impedance varies dramatically with input code. Due to the nature of the R-2R ladder, even small changes in the DAC output voltage can cause a step change of 1mA or more in the reference current. For this
reason, the reference must be buffered by a high-performance amplifier using a careful force-
sense board layout to limit the resulting degradation of settling, glitch impulse, and linearity.

When an output buffer amplifier is used with a voltage output R-2R DAC, the open loop gain and large signal common-mode rejection of the amplifier must be high enough to maintain the linearity of the output (>110dB at 18 bits). The offset and input bias current of the output buffer will appear primarily as offset at the DAC output, but any variation in these parameters over the input common-mode range will appear as an additional INL error.

Note that it is necessary to maintain matched impedances between the positive and negative reference switches to preserve the DAC linearity. Since CMOS switch impedance is a strong function of voltage and temperature, this presents a challenge for precision DACs, particularly at low supply voltages. The PSRR of available 18-bit DACs using this architecture is limited to about 64dB. As a result, the power supply must be held constant to within about 0.5% over time, temperature, line, and load conditions to maintain 18-bit performance. The INL of such DACs can be expected to drift by ±0.5LSB or more over the operating temperature.

To date 18-bit DACs using this architecture with an integrated output amplifier have been limited to ±2LSB INL at 18 bits using a 5V supply. At 3V performance is further limited to ±3LSB INL at 18 bits and monotonicity is reduced to 17 bits.

**Current-Output R-2R DACs**

An alternative configuration of a resistive ladder DAC uses terminal C in Figure 2 as the reference and connects terminal B to ground. Terminal A is connected to the negative feedback pin of the output amplifier. As the legs of the resistive ladder switch between A and B, current is steered across the feedback resistor to generate the DAC voltage at the amplifier output.

This architecture offers many advantages for high-precision applications. The reference impedance is constant and can be driven with an unbuffered reference or a slow low-precision op amp. Since both terminals A and B are at the same ground potential, it is relatively easy to maintain matched switch impedances, even in the presence of varying supply voltage and temperature. As a result, precision current-output R-2R DACs are available with excellent PSRR and temperature drift.

The output amplifier used with a current-output R-2R DAC requires high open loop gain (>110 dB at 18 bits) and low-offset voltage. Any offset between terminals A and B will generate a code dependent error current, which will appear as an INL error. The input bias current of the output buffer is less critical, and appears primarily as an offset at the DAC output. Since both inputs are always at ground, the common-mode rejection of the amplifier is not critical.

Current-output R-2R DACs that achieve ±1LSB INL at 16 bits have long been widely available, and a new family of 18-bit DACs from Linear Technology achieves ±4 ppm accuracy or ±1LSB max INL at 18-bit resolution, guaranteed over the full temperature range (Figure 3). The LTC2757 offers a parallel interface and is available immediately. The LTC2756/8 single and dual SPI DACs are planned for release within the next few months.
The LTC2757 INL drift from -40°C to +85°C is typically less than ±0.2LSB at 18 bits, and the high 96dB PSRR renders the output insensitive to supply variation.

![INL Drift Graph](image)

**Figure 3:** The LTC2757 18-bit DAC (Figure 3a) offers ±1LSB Max INL and DNL guaranteed from -40°C to +85°C and (Figure 3b) settles from a 10V step to within 1LSB in 2.0µs.

**Buffered Versus Unbuffered DAC Outputs**

Some high precision DACs integrate the output amplifier inside the DAC, while others require an external op amp. In both cases, most DACs offer integrated level-shift and feedback resistors to eliminate the need for precision external components. The primary advantages of integrated output amplifiers are footprint and convenience. Cost is usually not a dominant factor, since external amplifier components are normally much cheaper than the DAC itself.

Designers should be aware that an integrated output amplifier may compromise design flexibility. The combination of output swing, speed, noise, and power offered by the internal amplifier is unlikely to be optimal for a wide range of applications. For example, an integrated single-supply output amplifier will suffer degraded accuracy near the rails, so that designers must provide a level-shifted differential reference to use the full range of DAC codes. If the negative feedback input of an internal amplifier is not accessible, it may not be possible to compensate the output loop for large capacitive loads or add an external buffer without a second feedback loop. Users requiring a wider output swing or higher load current will suffer the accuracy, noise, and power penalty of an additional external amplifier stage with an independent feedback loop in series with the internal amplifier loop.

An unbuffered DAC with an external amplifier will normally achieve the best performance. The wide range of available components gives designers freedom to choose a solution with optimum precision, speed, noise, and power for a given application.
Choosing an Output Amplifier

Offset voltage is an important consideration when choosing an amplifier circuit for use with a precision current-output DAC such as the LTC2757. The sensitivity of the DAC linearity to amplifier offset is dependent on the DAC implementation, and should be described by the manufacturer in the data sheet. For the LTC2757, an offset voltage of ±80µV will result in about ±1LSB of INL error at the DAC output.

The simplest solution for best DC accuracy is to use a low-offset (<10µV) auto-zero amplifier such as the LTC1150 or LTC2054. For wider output swing, a second buffer amplifier such as the LT1010 can be incorporated in the loop. The LT1012 is a good intermediate output amplifier which achieves moderate speed (120µs settling) and good accuracy (±25µV offset) with low power (11.4mW).

For high speed applications a good choice is the LTC1468-2, which settles a 10V step to within ±1LSB at 18 bits in 2µs. Note that the ±75µV max offset will degrade the INL at the DAC output by up to ±0.9LSB. For high-speed applications demanding higher precision, the amplifier offset can be nulled with a digital potentiometer.

For best accuracy at high speed without offset nulling, a composite amplifier circuit is a good choice. For example, Figure 4 shows the LTC2054 used as an integrator to null the amplifier offset. During output slewing, the LTC6240 minimizes the disturbance at the input to the integrator to avoid disrupting the low frequency path. Note that any DC current across the 1kΩ resistor appears as an offset voltage and would cause INL error, so the low input bias current of the LTC6240 is important. The LTC1360 provides a wide output swing. The resulting composite amplifiers achieves 8µs settling with 16nV/√Hz noise density.

Figure 4: DAC output amplifier examples
Conclusion

Although numerous DAC architectures allow users to achieve 18 bits of resolution and monotonicity, resistive ladder or R-2R DACs are the best choice for users requiring better than ±15ppm accuracy, or ±1LSB INL at 16 bits. In choosing between voltage and current-output R-2R DACs, designers should be aware of the different requirements imposed on the supply, reference, and output amplifier by each architecture. Choosing an unbuffered DAC and combining it with a carefully chosen amplifier maximizes design flexibility and provides the optimal solution for a given application.